REMARKS

Claim 53 and 66 have been amended and claims 67-74 have been added. Claims 1-7 and 51-74 remain in the application. This Preliminary Amendment accompanies a Request for Continued Examination (RCE) Transmittal. Examination of the claims in this preliminary amendment is requested.

Claims 53 and 66 have been amended to address minor informalities noted during review, however, these amendments do not alter the scope of the claims.

Claims 1-7 and 51-66 stand rejected under 35 U.S.C. §102(e) as being anticipated by Forbes, U.S. Patent No. 5,897,351. The Examiner also asserts that "Claims stand rejected under 35 U.S.C. §103(a) as being unpatentable over Forbes, U.S. Patent No. 5,897,351." Applicants infer that the Examiner had intended to reject claims 52 and 53.

The §102 rejection of claims 1-7 and 51-66 is believed to be in error. Specifically, the PTO and Federal Circuit provide that §102 anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. *In re Spada*, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). The corollary of this rule is that the absence from a cited §102 reference of any claimed element negates the anticipation. *Kloster Speedsteel AB, et al. v. Crucible, Inc., et al.*, 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 1986).

To further delineate and clarify the legal meaning of the term "anticipation", Applicants note the requirements of MPEP §2131, which states

that "TO ANTICIPATE A CLAIM, THE REFERENCE MUST TEACH EVERY ELEMENT OF THE CLAIM." This MPEP section further states that "'A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."

Additionally, the reference must enable the claimed invention. This is explained in MPEP §2121.01, entitled "Use of Prior Art in Rejections Where Operability Is In Question". This MPEP section states that "In determining that quantum of prior art disclosure which is necessary to declare an applicant's invention 'not novel' or 'anticipated' within section 102, the stated test is whether a reference contains an 'enabling disclosure'... ." *In re Hoeksema*, 399 F.2d 269, 158 USPQ 596 (CCPA 1968). A reference contains an "enabling disclosure" if the public was in possession of the claimed invention before the date of invention.

The Examiner states (p. 2) that Forbes '351 teaches "forming a plurality of shallow trench isolation regions received within a substrate, the regions define active areas, with some widths being no greater than 1 um, at least

two being different (Fig. 3 and Col. 7, lines: 55-63)." The Examiner is mistaken on multiple grounds.

First, Fig. 3 shows a single active area ridge having a single width. Thus, Fig. 3 cannot possibly show a plurality of active areas, as recited in all of Applicant's independent claims.

Second, the passage appearing at col. 7, lines 55-63 is unrelated to Fig. 3. This passage describes Fig. 4F (see col. 7, line 58, for an unambiguous statement contained in Forbes '351 to this effect). In other words, the reference relied upon by the Examiner (on p. 2, and also on p. 3, first full paragraph) does not describe plural active areas on one substrate, and Forbes '351 makes no representation to that effect.

Put another way, the Examiner's statement (p. 3, first full ¶) that "howeveras [sic] cited by the Examiner Col. 7, lines 55-63 explicitly state "active areas"- in the plural sense. Applicant argues that Col.7 does not describe Fig.3- but it describes layer 300 (the active areas) found in Fig. 3." is in error. There is no representation anywhere in Forbes '351 regarding multiple active areas having different widths that are formed on a common substrate, as recited in each of Applicant's independent claims.

Third, Figs. 4A through 4F unambiguously show that the silicon bars 404 formed on any individual substrate have a single common width, in direct and stark contrast to the invention as recited in claim 1 ("forming a plurality of shallow trench isolation regions received within a substrate, the shallow trench isolation regions being formed to define a plurality of active areas having widths within the substrate, some of the widths being no greater than

about one micron, at least two of the widths being different"), claim 54 ("forming a plurality of shallow trench isolation regions received within a substrate, the shallow trench isolation regions being formed to define a plurality of active areas having widths over the substrate, at least two of the widths being different, at least one of the plurality of active areas having a width less than one micron") or claim 63 ("forming a plurality of shallow trench isolation regions received within a substrate, the shallow trench isolation regions being formed to define a plurality of active areas having widths within the substrate, some of the widths being no greater than about one micron, at least two of the widths being different").

In other words, each of Applicant's independent claims clearly and unambiguously recite that multiple active widths are formed on a substrate. Forbes '351 fails to teach or disclose any such thing.

Fourth, Forbes '351 does not teach shallow trench isolation. In fact, Forbes '351 is void of the word "shallow". In other words, the term "shallow" does not appear anywhere in Forbes '351.

Fifth, Forbes '351 teaches use of LOCOS techniques for isolation. See, e.g., col. 7, lines 55-63. Forbes '351 also teaches methods described at col. 6, line 30 through col. 8, line 37 to form silicon bars 404. Forbes also teaches that these may be formed using processes as described at col. 6, lines 47-62. These techniques are not shallow trench isolation, and Forbes certainly does not represent them as such.

Sixth, the terms "LOCOS" and "shallow trench isolation" are terms of art having specific and different meanings to those of ordinary skill in the

semiconductor arts. Copies of pp. 330-1 and 367-8, taken from S. Wolf, "Silicon Processing for the VLSI Era", copyright 1995, Lattice Press, Sunset Beach, CA, describing these two different technologies, are enclosed for the Examiner's convenience. Note in particular that the text on p. 367 contrasts these two technologies and further shows why these two technologies are not arbitrarily interchangeable. The definition of the term "shallow trench isolation" provided in Wolf also makes clear that the methods for isolation of silicon islands taught by Forbes '351 are not arbitrarily interchangeable with shallow trench isolation as recited in all of Applicant's independent claims.

The Examiner states (p. 3) that "Applicant makes an interesting argument that Forbes fails to teach "shallow trench isolation" , this inference means that Forbes teaches only the formation of deep trenches." The Examiner is mistaken, to the extent that the Examiner's statement makes any sense at all. Forbes teaches use of LOCOS for isolation (see, e.g., col. 7, lines 58 and 59). Forbes does not teach the use of any trenches for isolation, in contrast to the Examiner's statement to the extent that such can be understood at all.

Seventh, it is inappropriate to modify the teachings of a reference in attempting to make a valid anticipation rejection under 35 U.S.C. §102. This is explained more fully in MPEP §706.02.

In a subsection entitled "DISTINCTION BETWEEN 35 U.S.C. 102 AND 103", this MPEP section states that: "The distinction between rejections based on 35 U.S.C. 102 and those based on 35 U.S.C. 103 should be kept in mind. Under the former, the claim is anticipated by the reference. No

question of obviousness is present." In other words, no modification or inference is allowed in a determination of anticipation. Put another way, the identical invention must be described and enabled within the four corners of the reference to provide a valid finding of anticipation.

Eighth, substituting the silicon bar structures 404 taught by Forbes '351 for the shallow trench structures recited in all of Applicant's independent claims gives the term "shallow trench structure" a meaning repugnant to the normal meaning of the term.

Applicant notes the requirements of MPEP §608.01(o), entitled "Basis for Claim Terminology in Description". This MPEP section states that "The meaning of every term used in any of the claims should be apparent from the descriptive portion of the specification with clear disclosure as to its import; and in mechanical cases, it should be identified in the descriptive portion of the specification by reference to the drawing, designating the part or parts therein to which the term applies. A term used in the claims may be given a special meaning in the description. No term may be given a meaning repugnant to the usual meaning of the term.

The Examiner's arbitrary conflation of terms of art, including LOCOS, shallow trench isolation and deep trenches gives each of these terms meanings repugnant to the usual meanings of these terms as used by those of ordinary skill in the art. Such is improper and should be retracted.

The Examiner seems to be under the false impression that the term of art "shallow trench isolation" refers only to the depth of the trenches involved. Evidence for this is found on p. 3 of the Office Action. More specifically, the

Examiner states (p. 3) that "Forbes explicitly teaches "trench isolation". col.6, lines: 35-45 teaches that the depth of the trenches may equal to [sic] one micron or less (the width of the silicon bars). Wolf (the art cited by applicant to explain shallow trench isolation) teaches forming shallow trenches at a range between .3-.5 microns. Since Forbes teaches that the trenches may be less than one micron- it follows that Forbes does in fact teach shallow trench isolation. Furthermore, there is no obviousness issue present." The Examiner is mistaken on multiple grounds.

Forbes fails to describe such as shallow trench isolation (or "STI"). Wolfe points out clearly (§6.5, p. 367) that STI involves a number of steps, including oxide refill followed by planarization. As noted above, the term of art "shallow trench isolation" refers to more than just a trench depth. Forbes does not use this language and does not describe such processes.

Thus, the statement that "it follows that" is in error, constitutes modification of the reference and fails to comport to appropriate standards for examination. Additionally, such gives the term of art "shallow trench isolation" a meaning repugnant to the ordinary meaning of the term as used in the art and as evidence by Wolf.

Ninth, arbitrarily substituting the processes taught by Forbes '351 for the shallow trench isolation recited in Applicant's independent claims requires modification of the teachings of the reference. It is inappropriate to modify the teachings of a reference in attempting to find anticipation.

Tenth, Forbes '352 fails to show, teach, describe or discuss transistors having different channel widths, as erroneously alleged in the Office Action.

Channel width refers to the effective separation between the source and the drain of a transistor, and corresponds roughly to source-drain separation and acts as an upper bound for gate length. Figs. 4A through 4I and 6 each show a plurality of active areas formed on a substrate and all having identical widths.

The illustration of Forbes' Fig. 3 depicts a p-channel transistor and an n-channel transistor that are illustrated as having identical dimensions for both gate width and gate length. The use of merged p- and n-channel transistors by Forbes '351 is described at least in the Title, Field of the Invention, col. 2, lines 26-33; col. 3, lines 6-16; col. 4, lines 29-32 and 61-65; col. 6, lines 7-9 etc. Forbes '351 is silent with respect to multiple channel or active area widths on a single substrate and thus cannot possibly teach or disclose the invention as recited in any of Applicant's claims.

The Examiner states (p. 3) that "Applicant argues that LOCOS is not trench isolation- LOCOS (an oxide) is deposited in the shallow trenches which acts [sic] as an isolation region- the Applicant's argument that the Examiner is replacing trench formation with oxide deposition techniques is unmerited." To the very limited extent that these statements make any sense at all in the English language, the Examiner is wide of the mark. In other words, the Examiner is mistaken on multiple grounds.

Applicants have provided the Examiner with technical information describing both techniques. LOCOS, once again, is an acronym derived from LOcal Oxidation of Silicon, with the underlined and capitalized letters forming the acronym. This technique has nothing to do with deposition of oxide.

LOCOS uses a deep oxidation of the silicon substrate itself to provide what is known in the art as a Field OXide or "FOX". No trenches are formed or involved in LOCOS.

Trench isolation techniques, on the other hand, involve formation of a trench followed by deposition of silicon dioxide. Applicants claim such a process in conjunction with other aspects of the invention. As noted above and in the last response, these techniques are not arbitrarily interchangeable.

Applicant is simply pointing out that Forbes does not teach any form of trench isolation, as recited in Applicant's claims, and instead teaches a different conventional isolation technique known as LOCOS.

As a result, Forbes fails to teach or disclose, or provide enabling disclosure for, or suggest or motivate, the invention as recited in any of Applicant's claims.

Accordingly, and for at least these reasons, the anticipation and unpatentability rejections of claims 1-7 and 51-66 are clearly in error and should be withdrawn, and claims 1-7 and 51-66 should be allowed.

Dependent claims 2-7, 51-53, 55-62 and 64-66 are allowable as depending from allowable base claims and for their own recited features which are neither shown nor suggested by the prior art.

Additionally, the Examiner's response to argument is deficient in multiple regards. A first deficiency is that the response to argument clearly fails to respond to all of Applicant's arguments with respect to the rejections under 35 U.S.C. §102, or, in the alternative, is an admission that these rejections are defective.

Applicants note the requirements of MPEP §707.07, entitled "Completeness and Clarity of Examiner's Action". This MPEP section cites 37 CFR §1.104, entitled "Nature of examination" which in turn states, in subsection (b), entitled "Completeness of examiner's action" that "The examiner's action will be complete as to all matters, except that in appropriate circumstances, such as misjoinder of invention, fundamental defects in the application, and the like, the action of the examiner may be limited to such matters before further action is made."

This MPEP section further states, under a heading labeled "Examiner Note" that "The Examiner must, however, address any arguments presented by the applicant which are still relevant to any references being applied." The Office Action clearly fails to comport with these requirements as set forth in the MPEP, at least because the Office Action both fails to address Applicant's arguments with respect to anticipation and continues to reject claims as being anticipated.

A second deficiency is that even under the unpatentability rejections, the combinations fail to provide all of the features recited in any of Applicant's independent claims. The Examiner has ignored these features without providing any appropriate legal basis for doing so.

A third deficiency is the failure to respond to all arguments traversing the unpatentability rejections. Merely repeating that "it would be obvious" to provide the features recited in the claims does not constitute a basis for rejection of the claims, particularly when the references fail to provide the

features recited in the claims and the rejections fail to meet the standards for such rejections as set forth in the MPEP and as demonstrated by Applicant.

For at least these reasons, the Office Action fails to comport with appropriate standards for examination. The Examiner should either allow Applicant's claims or provide a meaningful basis for rejection and an appropriate response to Applicant's arguments.

Further, Applicant herewith submits a duplicate copy of the Information Disclosure Statement and Form PTO-1449 filed in this application on June 11, 2001. No initialed copy of the PTO-1449 has been received back from the Examiner. To the extent that the submitted reference listed on the Form PTO-1449 has not already been considered, and the Form PTO-1449 has not been initialed with a copy being returned to Applicant, such examination and initialing is requested at this time, as well as return of a copy of the initialed Form PTO-1449 to the undersigned.

New claims 67-74 are similar to claims 1-7 but differ in scope. New claims 67-74 are supported by text appearing at p. 5, line 8 through p. 11, line 19 of the specification as originally filed. No new matter is added by new claims 67-74.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "**Version with markings to show changes made**."

In view of the foregoing, allowance of claims 1-7 and 51-74 is requested. The Examiner is requested to phone the undersigned in the event that the next Office Action is one other than a Notice of Allowance. The

undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: Oct. 31, 2001

By: _____

Frederick M. Fliegel, Ph.D.
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Version with markings to show changes made

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/388,857
Priority Filing Date .....September 1, 1999
Inventor .....Luan C. Tran
Assignee ..... Micron Technology, Inc.
Priority Group Art Unit 2813
Priority Examiner .....L. Schillinger
Attorney's Docket No. MI22-878
Title: Semiconductor Processing Methods Of Forming Transistors, Semiconductor Processing Methods Of Forming Dynamic Random Access Memory Circuitry, And Related Integrated Circuitry

37 CFR §1.121(b)(1)(iii) AND 37 CFR §1.121(c)(1)(ii)
FILING REQUIREMENTS TO ACCOMPANY
RESPONSE TO JULY 31, 2001 FINAL OFFICE ACTION
PRELIMINARY AMENDMENT TO ACCOMPANY RCE FILING

Deletions are bracketed, additions are underlined.

In the Claims

53. (Amended) The method of claim 1, wherein forming individual transistors comprises forming at least [two] three individual transistors, a first of the three having a first threshold voltage, a second of the three having a second threshold voltage greater than the first threshold voltage and a third of the three having a third threshold voltage greater than the second threshold voltage, the three individual transistors being configured to be coupled in parallel.

66. (Amended) The semiconductor processing method of claim [1] 63, wherein the at least two different widths are less than one micron, and the different threshold voltages are less than 1 volt.

Claims 67-74 have been added.

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